Amendments To The Claims

This list of claims replaces all prior versions and listings of claims in this application. Please cancel claims 2 and 5-10, add new claims 11-24 and amend claims 1 and 3-4, wherein strikethrough and double brackets indicates a deletion and underlining indicates additions, as follows:

1. (Currently Amended) A method of operating a dynamic random access memory (DRAM) using a bit line and a bit line bar, wherein a charge storage device of the DRAM is adapted for storing data~~, the charge storage device~~ and is coupled to the bit line via a switch device, the method comprising:

programming the charge storage device with ~~a first or a zero voltage, wherein when the switch device is turned on, a switch voltage drop generated in the switch device, and the first voltage equals to a voltage obtained by subtracting the switch voltage drop from a power voltage~~ a data status of a first status or a second status; and

accessing the data stored in the charge storage device, ~~wherein the step of~~ accessing the data ~~comprises~~ comprising:

~~charging the bit line and the bit line bar to the power voltage~~ providing the bit line and the bit line bar with an initial bias, wherein the bit line has a first-status bias when the bit line is coupled to the charge storage device in the first status and the bit line has a second-status bias when the bit line is coupled to the charge storage device in the second status;

providing the bit line bar with a sensing bias approximately when the bit line is coupled to the charge storage device, wherein the sensing bias is different from the initial bias of the bit line and is between the first-status bias and the second-status bias;

~~turning on the switch device,~~ coupling the bit line with the charge device to obtain a read-out level at the bit line; and

~~determining the data stored in~~ identifying the data status of the charge storage device ~~according to a voltage difference between the bit line and the bit line bar~~ by comparing the read-out level with the sensing bias.

2. (Cancelled)

3. (Currently Amended) The operating method ~~of DRAM~~ of claim [[2]] 1, ~~wherein the preset voltage is about one half of the voltage drop on the bit line while the switch device is turned on after the charge storage device is programmed by the zero voltage~~ wherein the sensing bias is equal to or approximates a level of the first status bias minus one-half of the voltage difference between the first status bias and the second status bias.

4. (Currently Amended) The operating method of ~~DRAM of~~ claim 1, wherein coupling the bit line with the charge device to obtain the read-out level at the bit line comprises turning on a switch device controlled by a word line, the switch being coupled with the storage device~~, and the word line turns on the switch device with the power voltage~~.

5-10. (Cancelled)

11. (New) The operating method of claim 1, wherein the first status equals to or approximates a ground-level voltage.

12. (New) The operating method of claim 1, wherein the second status approximates or is slightly lower than a power-level voltage.

13. (New) The operating method of claim 1, wherein the initial bias equals to or approximates a power-level voltage.

14. (New) The operating method of claim 1, wherein the dynamic random access memory (DRAM) is operated without using a charge pump.

15. (New) The operating method of claim 1, wherein the first-status bias approximates the initial bias minus a voltage drop from the initial bias to the first-status bias caused by the charge storage device in a logic 0 state.

16. (New) The operating method of claim 1, wherein the first-status bias approximates the initial bias minus a voltage drop from the initial bias to the first-status bias caused by the charge storage device in a logic 1 state.

17. (New) A method of accessing a dynamic random access memory (DRAM) having a bit line and a bit line bar, wherein a charge storage device of the DRAM is adapted for storing a data status of one of a first status or a second status, the method comprising:

providing the bit line and bit line bar with an initial bias, wherein the bit line has a first-status bias when the bit line is coupled to the charge storage device in the first status and the bit line has a second-status bias when the bit line is coupled to the charge storage device in the second status;

providing the bit line bar with a sensing bias approximately when the bit line is coupled to the charge storage device, wherein the sensing bias is between the first-status bias and the second-status bias;

coupling the bit line with the charge device to obtain a read-out level at the bit line;

identifying the data status of the charge storage device by comparing the read-out level with the sensing bias.

18. (New) The accessing method of claim 17, wherein coupling the bit line with the charge device to obtain the read-out level at the bit line comprises turning on a switch device controlled by a word line, the switch being coupled with the storage device.

19. (New) The accessing method of claim 17, wherein first status equals to or approximates a ground-level voltage.

20. (New) The accessing method of claim 17, wherein the second status approximates or is slightly lower than a power-level voltage.

21. (New) The accessing method of claim 17, wherein the initial bias equals to or approximates a power-level voltage.

22. (New) The accessing method of claim 17, wherein the sensing bias is different from the initial bias and the sensing bias equals to or approximates a level of the first status bias minus about one-half of the voltage difference between the first status bias and the second status bias.

23. (New) The operating method of claim 17, wherein the first-status bias approximates the initial bias minus a voltage drop from the initial bias to the first-status bias caused by the charge storage device in a logic 0 state.

24. (New) The operating method of claim 17, wherein the first-status bias approximates the initial bias minus a voltage drop from the initial bias to the first-status bias caused by the charge storage device in a logic 1 state.